M20001

High Bandwidth Dual 2:1 Mux/DeMux Passive Switch

The M20001 is a high bandwidth, low power, dual differential single pole, double throw switch. Both switches are controlled using a single select pin. Due to the very high bandwidth of the device, it can be used for routing and switching of very high-speed NRZ data.

The M20001 is offered in an industry standard, green and RoHS compliant, 3 mm x 3 mm QFN package. The device pinout is architected to enable optimized PCB routing while providing maximum crosstalk isolation. Crosstalk isolation is critical for successful data transmission at multi-gigabit speeds.

The M20001 operates from a single 3.3 V power supply. This supply is used to operate the switch control only, therefore, the M20001 consumes less than 2 mW of power during normal operation.

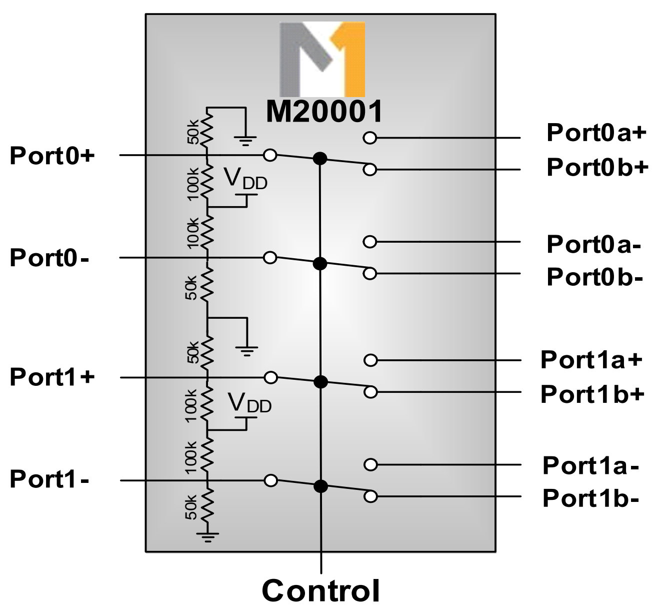
Features

- Two differential, single pole, double throw switches
- Low insertion loss
- 6 GHz 3 dB bandwidth
- Very low power consumption
- Superior crosstalk isolation
- 3 x 3 mm, 16-pin QFN package
- 3.3 V supply voltage, no additional regulation needed
- Industrial temp range -40 to 85 °C

Applications

- 10G Ethernet
- PCI Express Gen 3 — 8.0 Gbps
- SAS/SATA
- DisplayPort 1.2 — 5.4 Gbps
- USB 3.0 — 5 Gbps
- 3G SDI
- FibreChannel - 8.5 Gbps

Switch Control Diagram and Typical Application Diagram



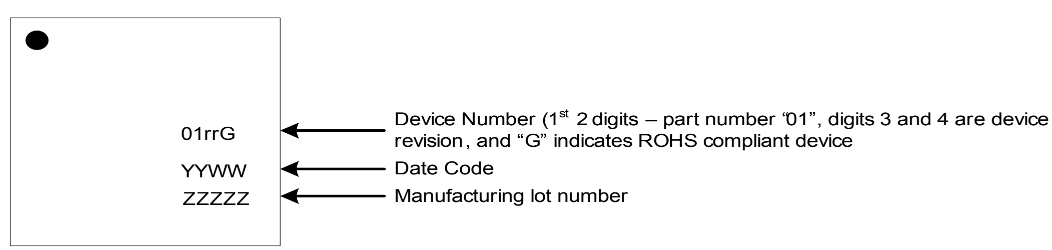
Ordering Information

Part Number	Package	Operating Case Temperature
M20001G-14*	3x3 mm, 16-pin QFN package	-40 °C to 85 °C
* The letter “G” designator after the part number indicates that the device is RoHS compliant. Refer to www.mindspeed.com for additional information. The RoHS compliant devices are backwards compatible with 225 °C reflow profiles.		

Revision History

Revision	Level	Date	Description
E	Advance	January 2014	Updated Front page Applications
D	Advance	April 2013	Updated specifications in Table 1-3 and Table 1-4. Revised Figure 1-1.
C	Advance	February 2012	Updated Ordering Information (added 13P). Table 1-1: $V_{ESD, HBM}$ maximum updated to 2000 V. Removed $V_{ESD, CDM}$ and $V_{ESD,}$ mm. Table 1-3: I_{DD} maximum updated to 600 μA; P_{TOTAL} maximum updated to 2.2 mW. Table 1-4: $t_{SKEW, PN}$ typical updated to 5 ps. Δ_{RON} typical updated to 0.55 Ω. $\Delta_{RON, CH}$ typical updated to 0.45 Ω. Removed I_{OUT_SHORT} and V_{OUT_OPEN}. Chapter 2: Updated all Insertion/Return Loss charts.
B	Advance	April 2011	Revised product title.
A	Advance	January 2011	Advance release.

M20001 Marking Diagrams



NOTE: Early device samples may be labeled as AP and BP to identify early lot numbers , lot number identified as A or B and “P” for prototype

1.0 Electrical Characteristics

Unless noted otherwise, test conditions in this section are: V_{DD} = 3.3 V, 25 °C case temperature, 800 mV differential input data swing ($V_{IH, DATA}$ = 200 mV), nominal (800 mV_{PPD}) output swing, PRBS 2^7- 1 test pattern with R_{LOAD} = 50 Ω, short traces and/or cables.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
V_{DD}	Supply voltage		-0.5	—	4	V
T_{STORE}	Storage temperature		-65		150	°C
$V_{ESD, HBM}$	Electrostatic discharge voltage (HBM)		—	—	2000	V
I_{SW}	DC current on data pins		—	—	4	mA

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
V_{DD}	Supply voltage	—	2.97	3.3	3.63	V
T_{CASE}	Operating case temperature	—	-40	—	85	°C
I_{SW}	DC current on data pins		—	—	3	mA

Table 1-3. Power Consumption Specifications

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
I_{DD}	Quiescent power supply current	—	—	100	500	μA
P_{TOTAL}	DC power consumption	—	—	0.33	1.8	mW

Table 1-4. Input/Output Electrical Characteristics

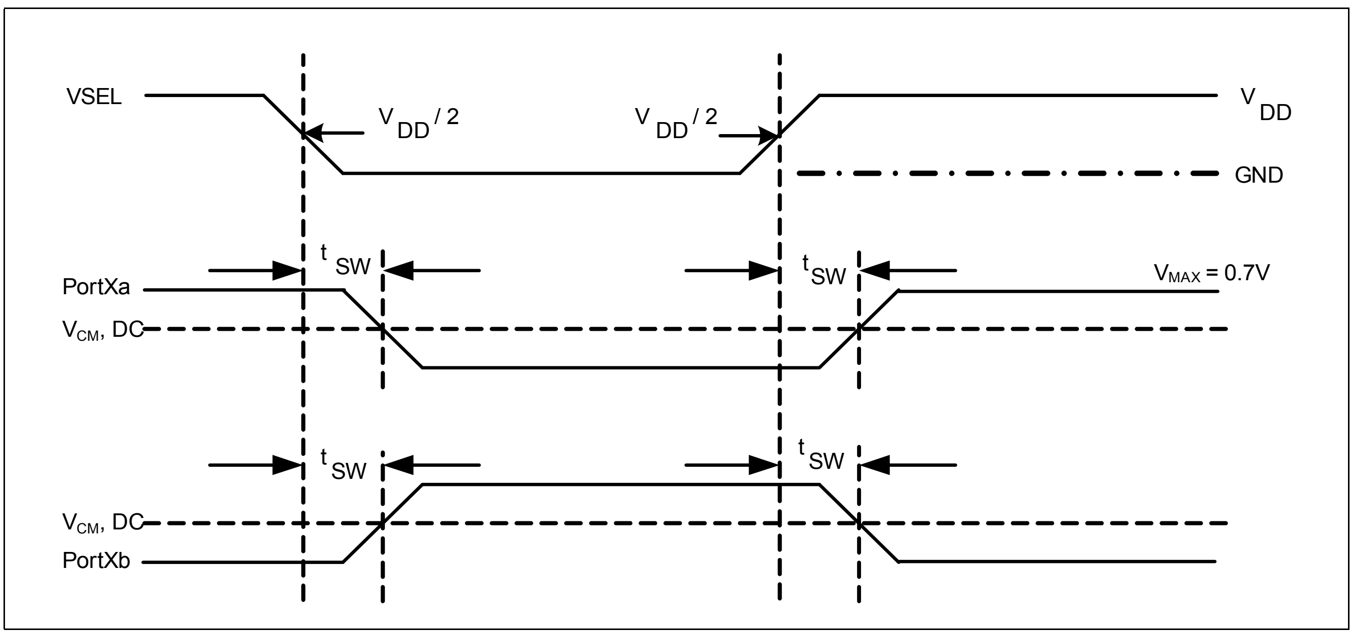
Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage on VSEL pin	1	0.7 x V_{DD}	—	V_{DD}	V
V_{IL}	Input low voltage on VSEL pin	1	0	—	0.3 x V_{DD}	V
V_{PPD}	Differential peak to peak input data swing (AC-coupled)	—	—	—	2.8	V
$V_{IH, DATA}$	Input high voltage on data pins, V_{PEAK}, AC-coupled	—	—	—	700	mV
$V_{CM, DATA}$	Common-mode voltage on data pins if DC-coupled (V_{DD}/3)	—	0.99	1.1	1.21	V
SW	Switching time	1	—	0.3	0.5	μs

Table 1-4. Input/Output Electrical Characteristics

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
$t_{SKEW, PN}$	Bit-to-bit skew within the same differential pair		—	8	15	ps
$t_{SKEW, CH}$	Channel-to-channel skew		—	12	25	ps
BW	3 dB bandwidth		5.6	6	—	GHz
X_{TALK}	Crosstalk 0 - 6 GHz (Port 0 to Port 1)		—	-30	-25	dB
OIRR	Off Isolation 0 - 6 GHz (PortX to PortXa with PortXb enabled)		24	26	—	dB
SDD21	Insertion loss @ DC		—	0.7	1.25	dB
SDD11	Differential return loss 50 MHz - 1.25 GHz		12.5	14	—	dB
SDD11	Differential return loss 1.25 GHz - 2.5 GHz		8	9	—	dB
SDD11	Differential return loss 2.5 GHz - 4 GHz		5	8	—	dB
SCM11	Common mode return loss 50 MHz - 2.5 GHz		12	14	—	dB
SCM11	Common mode return loss 2.5 GHz - 4 GHz		10.5	13	—	dB
RON	On resistance of the switch		—	8.5	15.5	Ω
Δ_{RON}	On resistance match between same pair		—	0.3	0.5	Ω
$\Delta_{RON, CH}$	On resistance match between channels		—	0.3	0.8	Ω

NOTES:
1. Control pin specifications.

Figure 1-1. Enable and Disable Timing Diagram



The timing diagram above shows the response of the high signal path when the VSEL pin is switched. When VSEL is set low PortXb will be disabled after time t_{SW} and PortXa will be enabled after time t_{SW}.

2.0 Typical Performance Characteristics

Unless noted otherwise, test conditions in this section are: V_{DD} = 3.3 V, 25 °C case temperature, 800 mV differential input data swing ($V_{IH, DATA}$ = 200 mV), nominal (800 mV_{PPD}) output swing, PRBS 2^7- 1 test pattern with R_{LOAD} = 50 Ω, short traces and/or cables, AC-coupled I/O.

Figure 2-1. Eye Diagram at 5 Gbps, 2 dB of De-emphasis

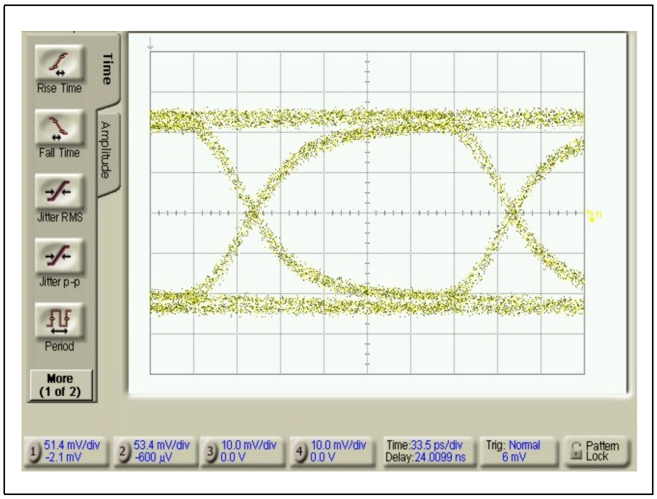


Figure 2-2. Eye Diagram at 8 Gbps, 2 dB of De-emphasis

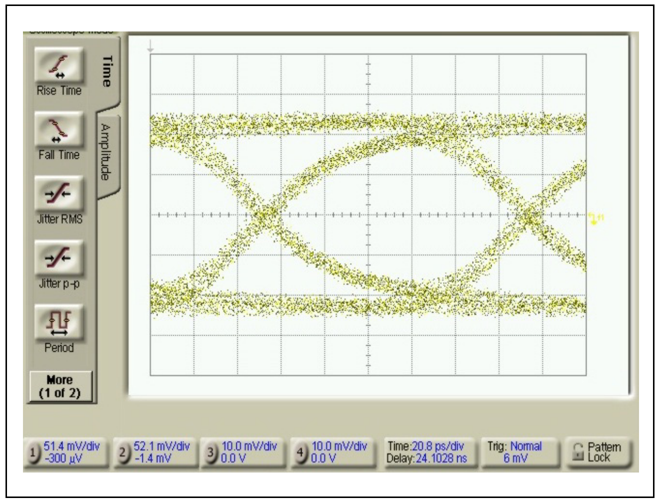


Figure 2-3. Eye Diagram at 10 Gbps, 2 dB of De-emphasis

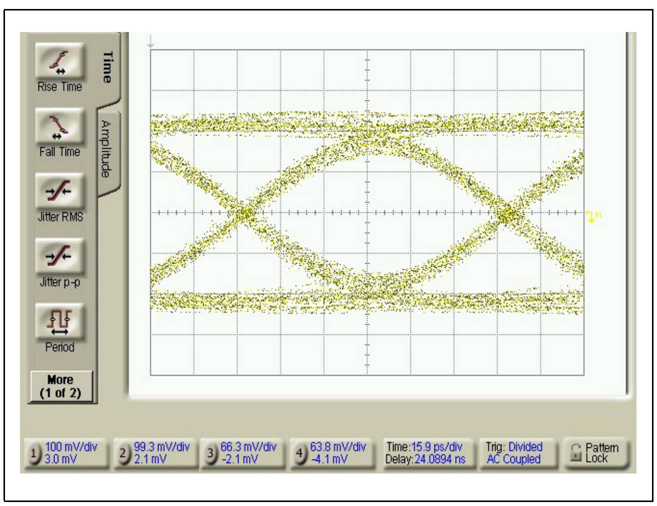


Figure 2-4. Eye Diagram at 12 Gbps, 2 dB of De-emphasis

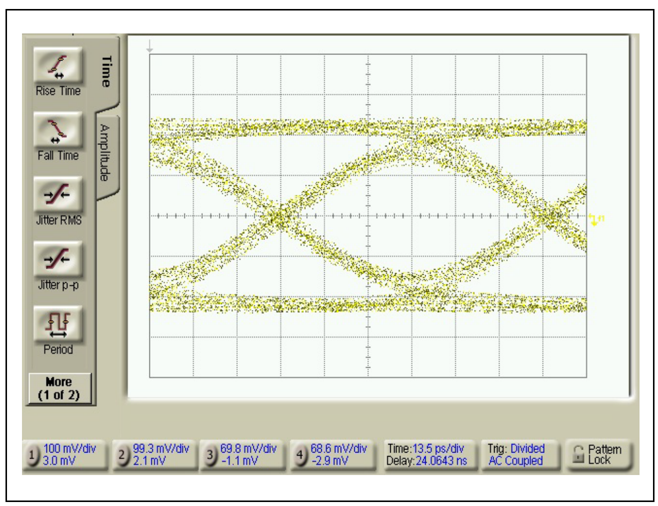


Figure 2-5. Insertion Loss as a Function of Temperature, Port 0 to Port 0b

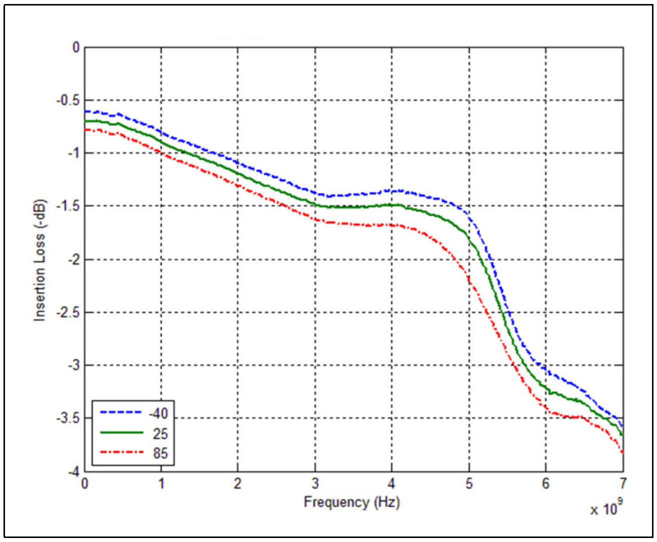


Figure 2-6. Insertion Loss as a Function of Supply Voltage, Port 0 to Port 0b

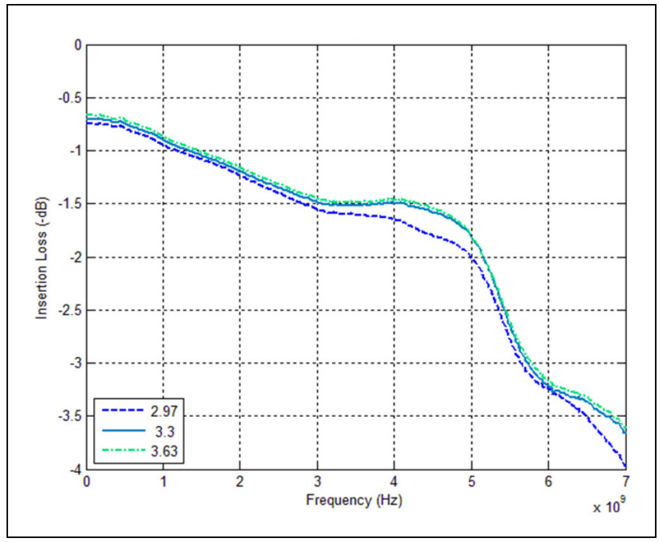


Figure 2-7. Return Loss as a Function of Temperature, Port 0 to Port 0b

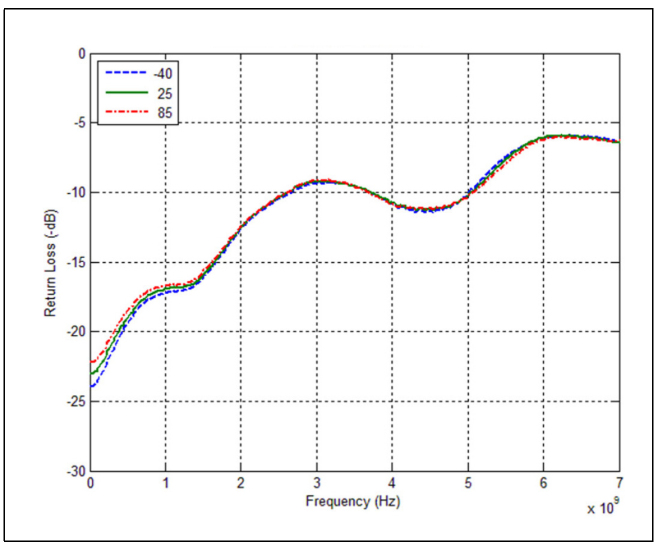


Figure 2-8. Return Loss as a Function of Supply Voltage, Port 0 to Port 0b

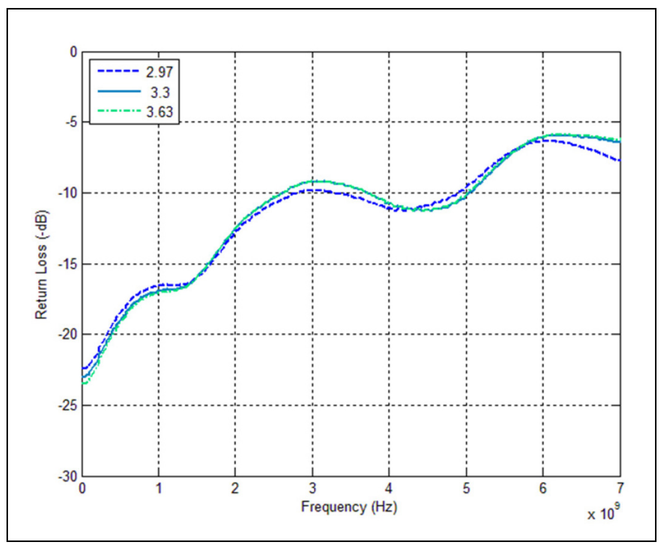


Figure 2-9. Insertion Loss as a Function of Temperature, Port 0 to Port 0a

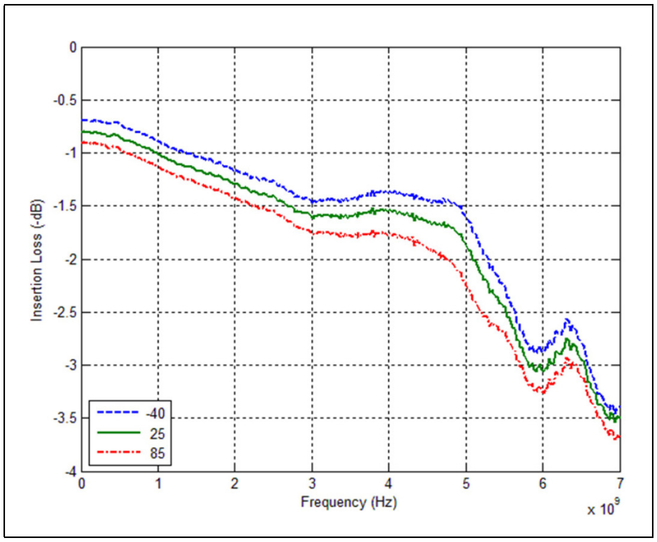


Figure 2-10. Insertion Loss as a Function of Supply Voltage, Port 0 to Port 0a

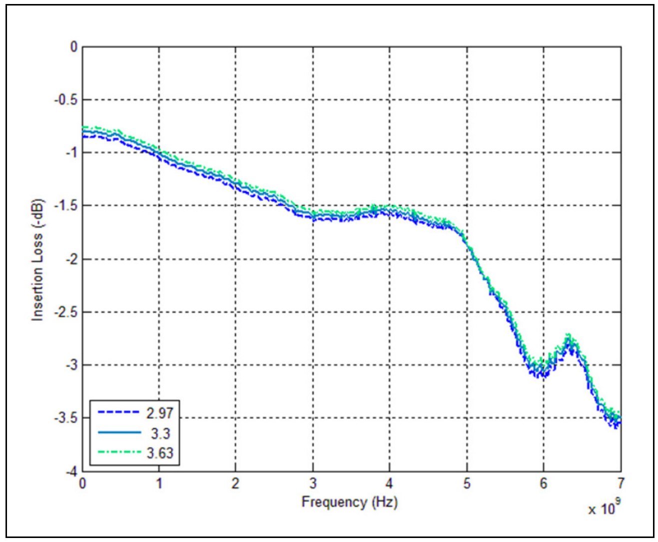


Figure 2-11. Return Loss as a Function of Temperature, Port 0 to Port 0a

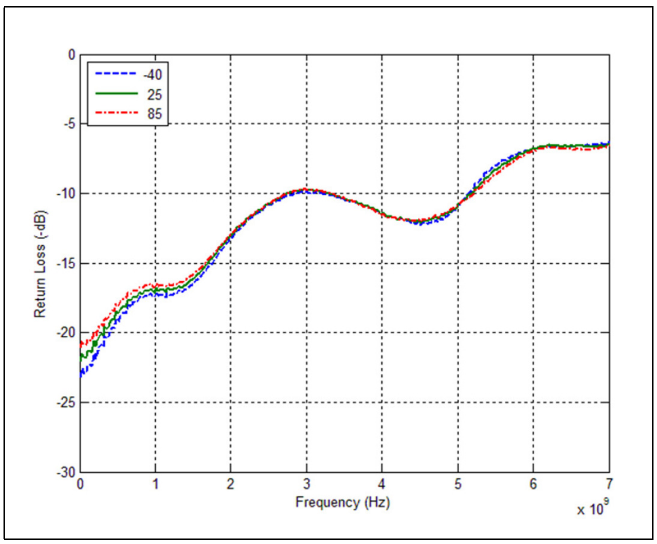


Figure 2-12. Return Loss as a Function of Supply Voltage, Port 0 to Port 0a

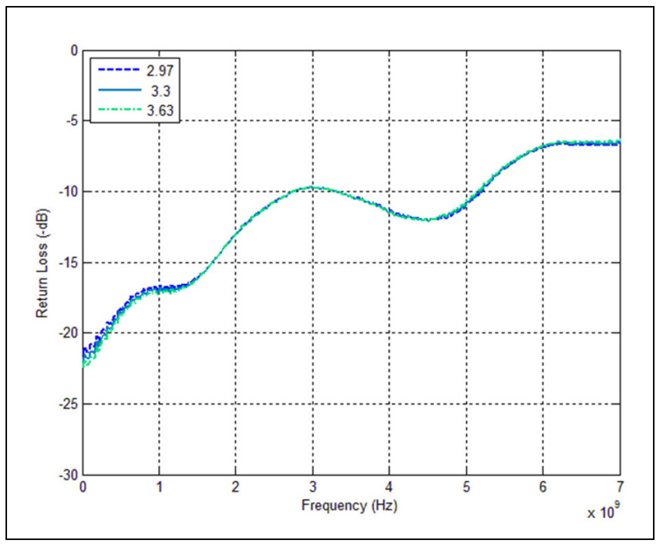


Figure 2-13. Insertion Loss as a Function of Temperature, Port 1 to Port 1b

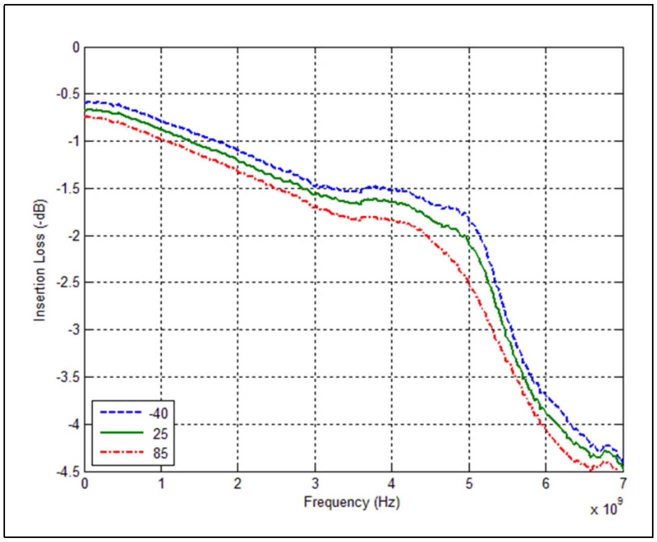


Figure 2-14. Insertion Loss as a Function of Supply Voltage, Port 1 to Port 1b

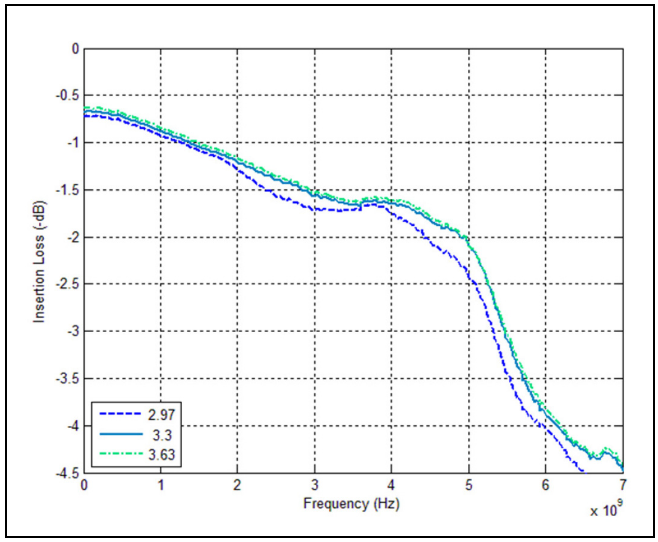


Figure 2-15. Return Loss as a Function of Temperature, Port 1 to Port 1b

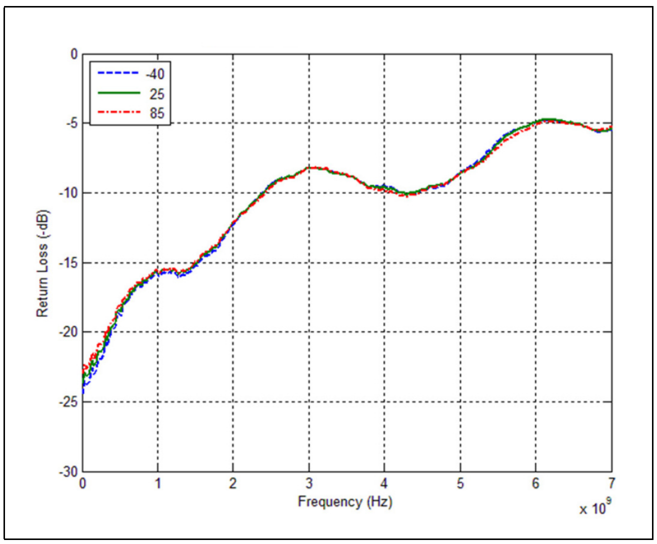


Figure 2-16. Return Loss as a Function of Supply Voltage, Port 1 to Port 1b

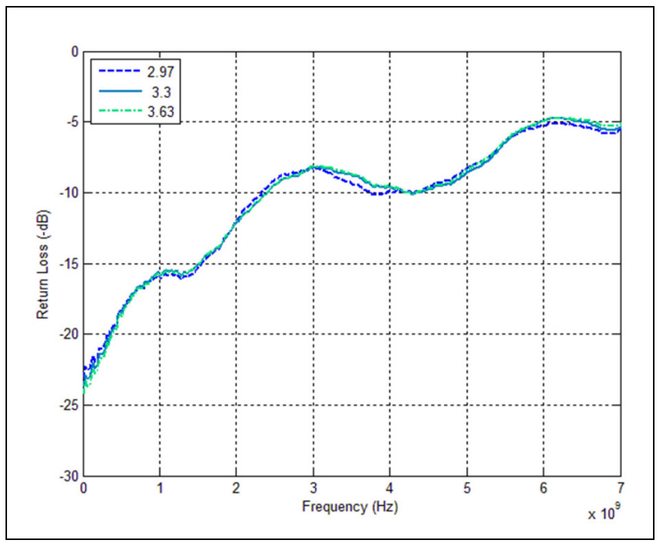


Figure 2-17. Insertion Loss as a Function of Temperature, Port 1 to Port 1a

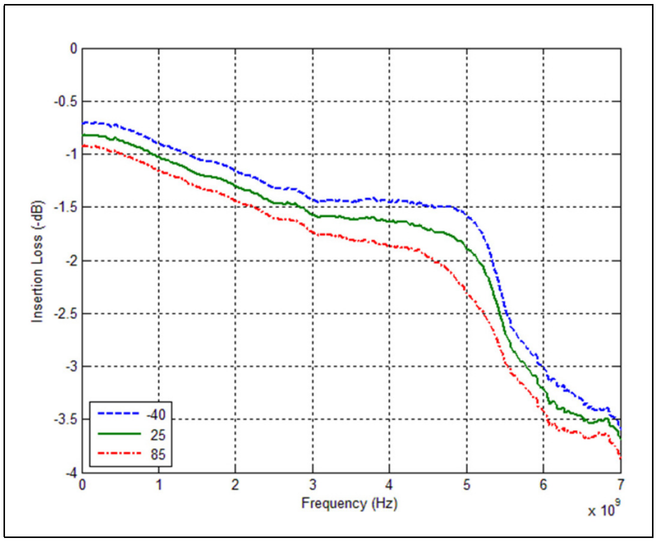


Figure 2-18. Insertion Loss as a Function of Supply Voltage, Port 1 to Port 1a

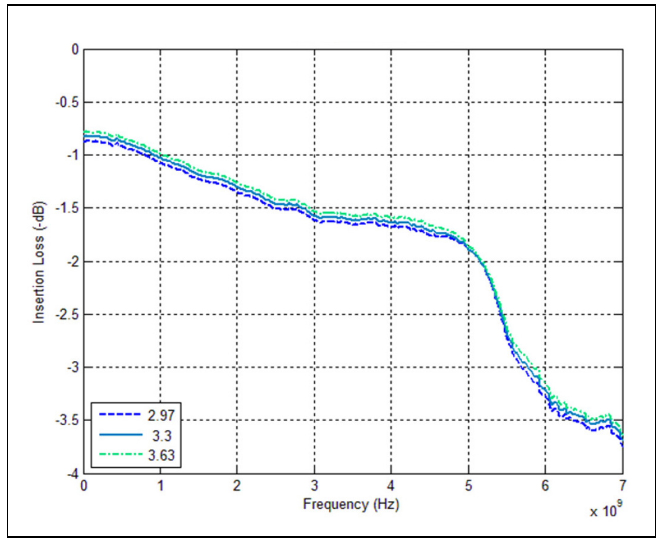


Figure 2-19. Return Loss as a Function of Temperature, Port 1 to Port 1a

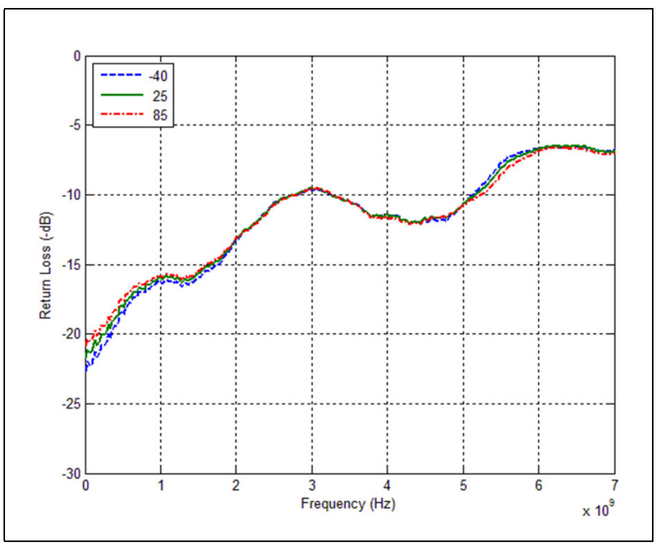


Figure 2-20. Return Loss as a Function of Supply Voltage, Port 1 to Port 1a

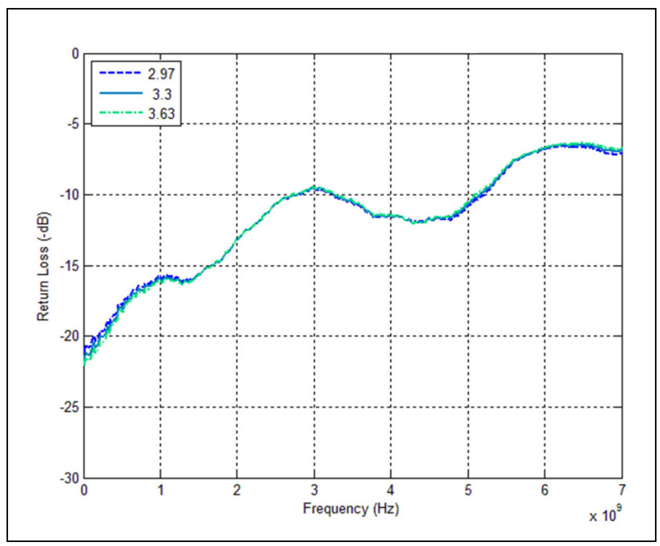


Figure 2-21. Isolation as a Function of Supply Voltage, Opposite Channels

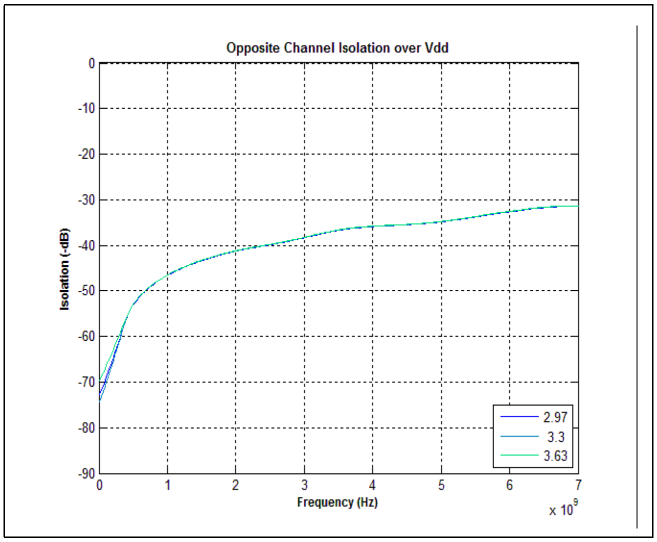


Figure 2-22. Isolation as a Function of Temperature, Opposite Channels

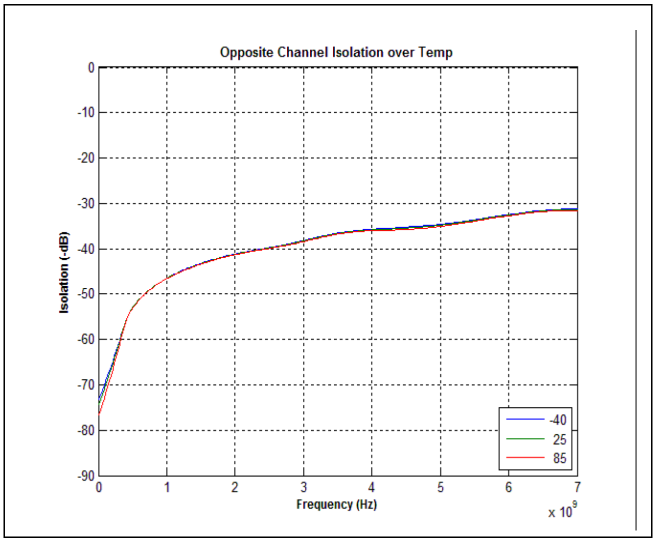


Figure 2-23. Isolation as a Function of Supply Voltage, Same Channels

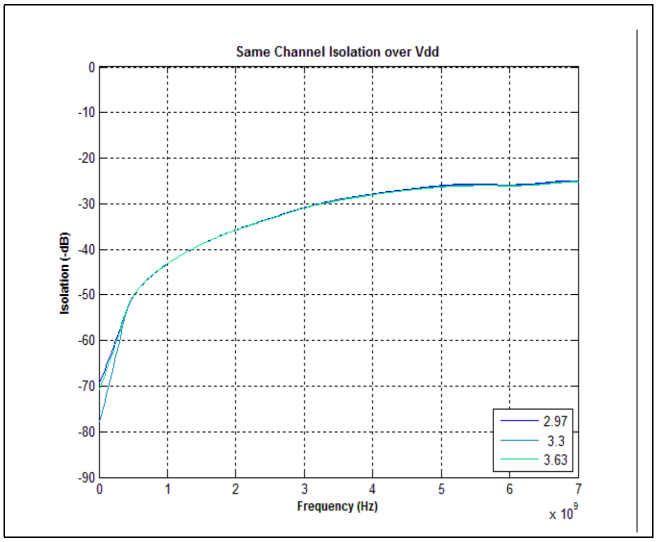
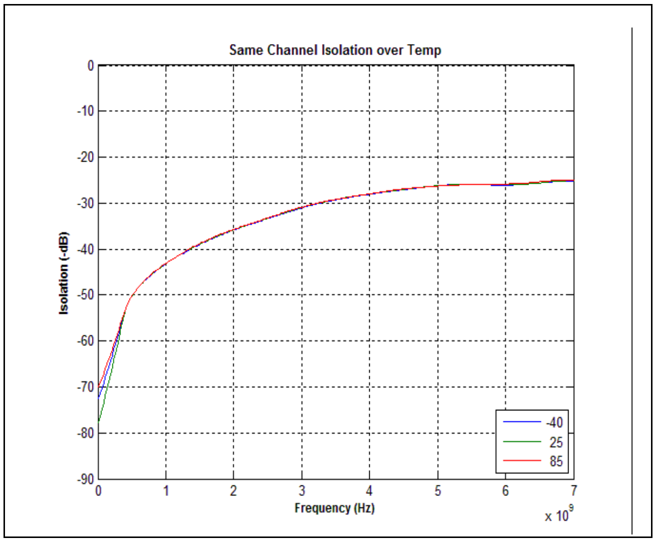


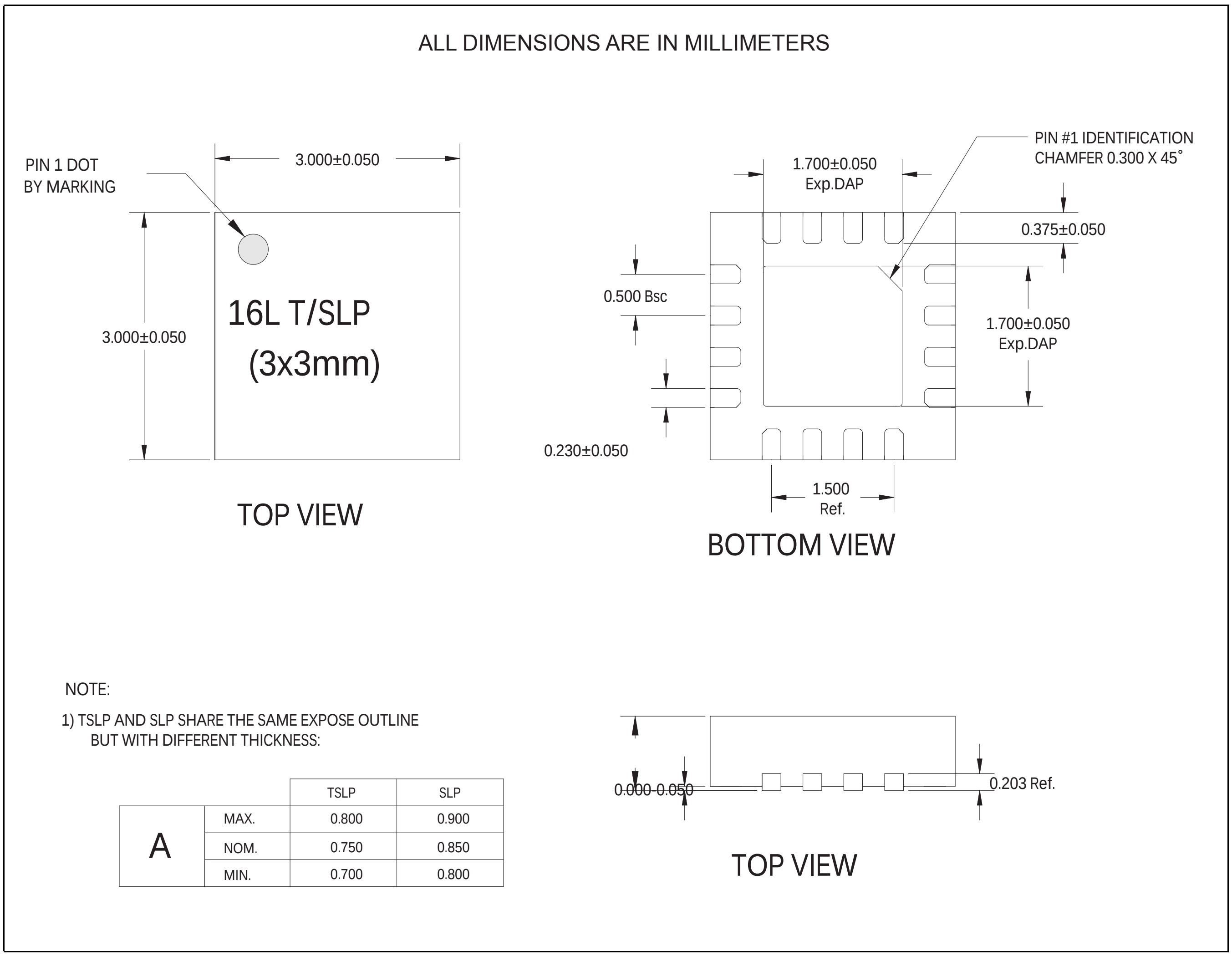
Figure 2-24. Isolation as a Function of Temperature, Same Channels



3.0 Pin Description, Pinout, and Package Outline Drawing

The M20001 is assembled in a 3 x 3 mm, 16-pin QFN package. The package paddle is used to provide the device ground connection as well as a thermal path.

Figure 3-1. M20001 Package Outline Drawing



		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

Figure 3-2. M20001 Pinout Diagram (Top View Shown)

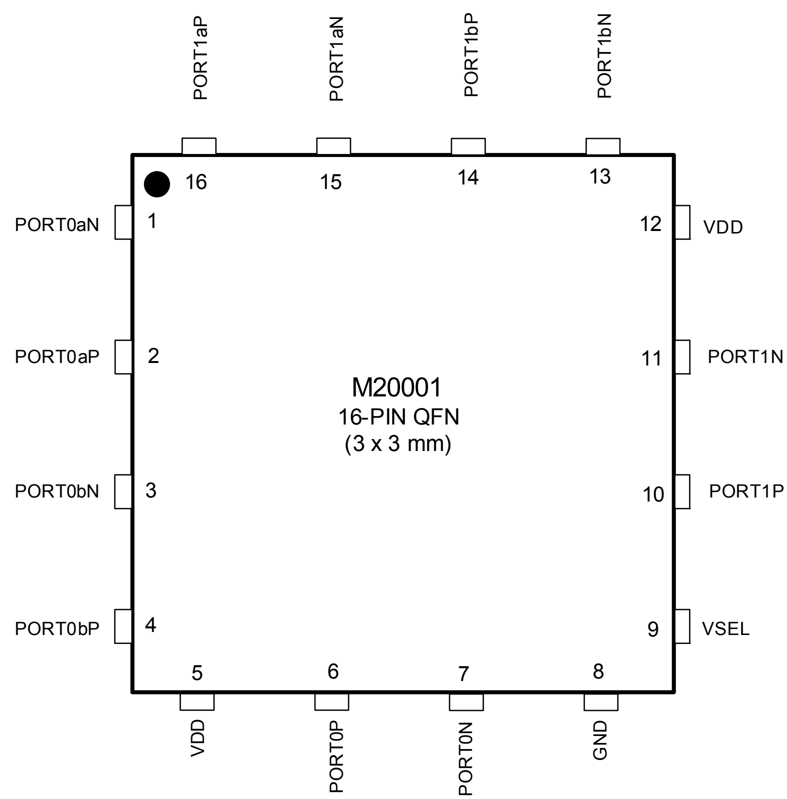


Table 3-1. M20001 Pin Descriptions

Pin Name	Pin Number(s)	Type	Description
PORT0aN	1	RF port	Analog switch 0a, N
PORT0aP	2	RF port	Analog switch 0a, P
PORT0bN	3	RF port	Analog switch 0b, N
PORT0bP	4	RF port	Analog switch 0b, P
V_{DD}	5, 12	Power	Positive supply voltage input
PORT0P	6	RF port	Analog switch 0, P
PORT0N	7	RF port	Analog switch 0, N
GND	8	Ground	Ground
VSEL	9	Control input	Control signal input: Low: Port A enabled High: Port B enabled
PORT1P	10	RF port	Analog switch 1, P
PORT1N	11	RF port	Analog switch 1, N
PORT1bN	13	RF port	Analog switch 1b, N
PORT1bP	14	RF port	Analog switch 1b, P
PORT1aN	15	RF port	Analog switch 1a, N
PORT1aP	16	RF port	Analog switch 1a, P

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